UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,632	04/02/2004	Anders Landin	5181-95501	2854

35690 7590 06/07/2006

MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
700 LAVACA, SUITE 800
AUSTIN, TX 78701

EXAMINER	
DOAN, DUC T	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 06/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/817,632	LANDIN ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-20 are in the application.

Claims 1-20 are rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-8,10-17,19-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US 5710907).

As in claim 1, Hagersten describes a system, comprising: a plurality of nodes, wherein each node includes an active device and a memory subsystem coupled to the active device (Hagersten's Fig 4); wherein an active device in a node of the plurality of nodes is configured to generate a global address and translation information identifying a translation function (Hargersten's Fig 3B, column 9 lines 17-32 describes the global address spaces coma/numa are

mapped to different address space ranges for different sub-systems #310,320,380; in coma mode, each subsystem uses the global address with translation function information, for looking up and translating to its local coma address space); wherein the global address identifies a coherency unit (Hargerten's column 9 lines 17-32 describes global address is used to identify a data unit in coma/numa coherency system); wherein a memory subsystem included in the node is configured to perform the translation function identified by the translation information on the global address to generate a physical address of the coherency unit within the memory subsystem (Hagersten's Fig 3B) ; wherein an additional memory subsystem included in an additional node of the plurality of nodes is configured to store the translation information identifying the translation function used in the node, wherein in response to a request for access to the coherency unit, the additional memory subsystem is configured to send the translation information to the node (Hagensten's Fig 3B, column 10 line 63 to column 11 line 7 describes if a "home node" does not have valid copy of the data line, then the request with the GA is forward to the address translator of the owner subsystem).

As in claim 2, Hagerten's describes wherein the plurality of nodes are coupled by an inter-node network, and wherein each of the plurality of nodes includes an interface to the inter-node network (Fig 2A); wherein an additional interface included in the additional node is configured to receive the translation information for the coherency unit from the additional memory subsystem (Fig 2A: 220 has interfaces #290 global interconnect, #229 local interconnect to receive and to translate address and data unit in a coma/numa coherency environment) ; wherein the additional interface is configured to provide the translation information and the global address to an interface included in the node via the inter-node network (Fig 2A: #227

address translation, #290 inter-node network) ; and wherein the interface included in the node is configured to provide the translation information and the global address received via the inter-node network to the memory subsystem (Fig 2A).

As in claim 3, the claim recites wherein the additional memory subsystem is configured to perform a different translation function on the global address to obtain a local physical address of the coherency unit within the additional memory subsystem (Hagersten's column 9 lines 17-31 describes different translation functions and algorithms are used for address translation in either coma or numa modes).

As in claim 4, the claim recites wherein the additional memory subsystem is configured to store translation information associated with the coherency unit for several other nodes included in the plurality of nodes, wherein different translation information is associated with each of the several other nodes. The claim rejected based on the same rationale as in the rejection of claim 3. Hagersten's Fig 3B, column 10 lines 30-40, line 62 to column 11 line 6 further shows a home node can translate/convert the global address space information and forwarding the request to the owner's node translator.

As in claim 5, Hagersten's describes wherein each active device included in the plurality of nodes is configured to use at least a portion of the global address of the coherency unit to determine whether a copy of the coherency unit is locally cached by that active device (Hagersten's Fig 3B column 10 lines 10-40, coma mode local coma address space).

As in claim 6, the claim recites wherein an additional active device in the additional node is configured to initiate a coherency transaction to gain access to the coherency unit by sending the request for access to the coherency unit to the additional memory subsystem, wherein the

request for access includes the global address and additional translation information, and wherein the additional translation information is associated with the coherency unit in the additional node;

wherein the additional memory subsystem is configured to send an packet indicating the coherency transaction to an additional interface included in the additional node, wherein the packet includes the global address and the translation information for the node (Hagersten's Fig 3B, column 10 lines 30-40, line 62 to column 11 line 6 further shows a home node can translate/convert the global address space information and forwarding the request to the owner's node translator),

wherein in response to the packet, the additional interface is configured to communicate the global address and the translation information to an interface included in the node.

The claim appears to describe the situation in which the home node not having the copy of the data, and sending out the request to the owner, in response to this request, the data will be sent to the requester node.

The claim rejected based on the same rationale as in the rejection of claim 1 and 4. Furthermore, Hagersten's Fig 3c, 3d, 3e shows the steps that are applicable to the processor "active device" in the "home node" received the sends the request to acquire a data unit, the request is translated to a global address, including translating information associating with the global coma/numa address space. Fig 2E step 3200), sending a request to the owner of the data (Fig 2E: #2152), in response the request data is returned to the requestor.

As in claims 7-8, the claims recite wherein no memory subsystem included in an other node of the plurality of nodes maps the global address, wherein an other active device included

in the other node is configured to request access to the coherency unit by sending a packet including the global address and translation information associated with the coherency unit in the other node on a network included in the other node, wherein the translation information associated with the coherency unit in the other node indicates that no memory subsystem included in the other node maps the coherency unit (claim 7); wherein an other interface included in the other node and coupled to the network is configured to forward the global address to an additional interface included in the additional node in response to receiving the packet (claim 8). Hagerten's column 10 lines 1-10 clearly teach that a node can operate in coma or numa mode. When it operates in numa mode, there is no need for the "attract cache" (corresponds to the claim's no memory subsystem included in the nodes' mapping) as required in coma node. The translation information would indicate the operation is in numa mode by using the information in the request's addresses.

Claim 10 rejected based on the same rationale as in the rejection of claim 1.

Claim 11 rejected based on the same rationale as in the rejection of claim 2.

Claim 12 rejected based on the same rationale as in the rejection of claim 3.

Claim 13 rejected based on the same rationale as in the rejection of claim 4.

Claim 14 rejected based on the same rationale as in the rejection of claim 5.

Claim 15 rejected based on the same rationale as in the rejection of claim 6.

Claim 16 rejected based on the same rationale as in the rejection of claim 7.

Claim 17 rejected based on the same rationale as in the rejection of claim 8.

As in claim 19 the claim recites an operating system executing on the active device creating a translation lookaside buffer entry corresponding to the virtual address, wherein the

translation lookaside buffer entry includes the global address and the information identifying the translation function, wherein the operating system selects the translation function in order to map the global address to the local physical address within the memory. Hagersten's column 3 lines 43-55 and column 4 lines 38-52 describes of using a cache in a node to store a copy of coherency data in this node beside the copy of data in the home node (in coma mode). Furthermore, it's well known fact that a MMU management unit includes a translation look aside buffer to maintaining frequently used translation values;

As in claim 20, the claim recites an operating system executing on the active device in the node creating a translation lookaside buffer entry corresponding to a virtual address in response to deciding to replicate the coherency unit to the node from the additional node, wherein the translation lookaside buffer entry corresponding to the virtual address specifies the global address and the information identifying the translation function. The claim rejected based on the same rationale as in the rejection of claim 19. Hagerten's Fig 3C further shows the data request/response will be present to a processor's program, and in conjunction with operating system and MMU and memory sub-system management units appropriated address translation and entries will be recorded in the directory for subsequent data referencing and address translation tasks. Furthermore, it's well known fact that a MMU management unit includes a translation look aside buffer to maintaining frequently used translation values.

Claims 9,18 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US 5710907) in view of Arimili et al (US 2002/0112124).

As in claim 9, the claim recites wherein a memory controller included in the memory subsystem is integrated in a same integrated circuit as the processing subsystem. Hagersten does not describe the claim's aspect of an integrated memory controller. However, Arimilli's paragraph 6 discloses a multiple processors system with integrated memory controller circuit. It would have been obvious to one of ordinary skill in the art at the time of invention to include integrated memory controller circuit as suggested by Arimilli in Hagersten's system to allow fast communication between the processor and the memory controller since they are located in the same chip (Arimilli's page 1 paragraph 6).

Claim 18 rejected based on the same rationale as in the rejection of claim 9.

As in claim 16, the claim recites an operating system executing on the active device creating a translation lookaside buffer entry corresponding to the virtual address, wherein the translation lookaside buffer entry includes the global address, wherein the operating system selects the translation function in order to map the virtual address to the local physical address within a non-replicated range of local physical addresses of the memory subsystem (Hagersten's Fig 3A MMU management unit converting virtual address to physical address. Furthermore, it's well known fact that a MMU management unit includes a translation look aside buffer to maintaining frequently used translation values; It's note that the mapped physical addresses are used in both coma and numa modes, and in numa mode, the data is not replicable).

As in claim 17, the claim recites the operating system executing on the active device in one of the nodes creating the translation lookaside buffer entry corresponding to the virtual

address in response to deciding to replicate the coherency unit to the node from an additional one of the plurality of nodes. The claim rejected based on the same rationale as in the rejection of claim 16. Its note that the mapped physical addresses are used in both coma and numa modes, and in coma mode, the data is replicable.

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Hagersten et al (US 2002/0019921) as applied to claim 1 and in view of Arimili et al (US 2002/0112124).

As in claim 8, the claim recites wherein a memory controller included in the memory subsystem is integrated in a same integrated circuit as the active device. Hagersten does not describe the claim's aspect of integrated memory controller. However, Arimilli's paragraph 6 discloses a multiple processors system with integrated memory controller circuit. It would have been obvious to one of ordinary skill in the art at the time of invention to include integrated memory controller circuit as suggested by Arimilli in Hagersten's system to allow fast communication between the processor and the memory controller since they are located in the same chip (Arimilli's page 1 paragraph 6).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Liberty (US 6275900).

Arimilli (US 2003/0009640).

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 4/24/04

DD

Mano Padmanabhan

Supervisory Patent Examiner

TC2188

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER